Three Rivers Community College
EET K254 – Digital Electronics I
Course Syllabus – Fall 2018

Instructor

Mr. Aaron Dahlen Office C-140 adahlen@trcc.commnet.edu

Course Description

Credit Hours: 3.0 Format: Class Prerequisite: *EET K105*; *MAT K137* or *MAT K137*

Students will engage in a comprehensive study of binary logic gates. The circuits for certain various gates are analyzed. The course also includes the study of codes, encoding, decoding, number systems, and various sequential logic circuits such as flip-flops, counters, and shift registers. Two hours lecture and three hours laboratory, course meets five hours per week. In the laboratory portion of the course, students will engage in a comprehensive study of logic circuitry. Circuits containing various logic gates are built and tested. Applications of logic circuitry in practical applications are also build and evaluated.

Class Time

Monday / Wednesday 01:30 PM - 02:20 PM and 02:21 PM - 03:36 PM in B213

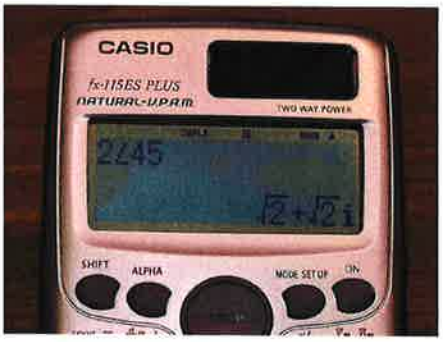
Office Hours

Scheduled hours posted on Blackboard, and office door; also available by appointment.

Required Materials

Textbook: Digital Design with RTL Design, VHDL, and Verilog 2nd Edition" by Frank Vahid ISBN-13: 978-0470531082

Calculator: An engineering / scientific calculator is required. The quizzes and exams are written assuming the student's calculator can quickly switch between number bases. The **Casio fx-115ES Plus** is recommended for this course. Cell phones are not allowed.



University Policy

Academic integrity policy / statement: Academic integrity is essential to a useful education. Failure to act with academic integrity severely limits a person's ability to succeed in the classroom and beyond. Furthermore, academic dishonesty erodes the legitimacy of every degree awarded by the College. In this class and in the course of your academic career, present only your own best work; clearly documenting the sources of the material you use from others; and act at all time with honor.

Student disabilities policy / statement: Three Rivers Community College (TRCC) is committed to the goal of achieving equal educational opportunity and full participation for individuals with disabilities. To this end, TRCC seeks to ensure that no qualified person is excluded from participation in, is denied the benefit of, or otherwise is subjected to discrimination in any of its programs, services, or activities. Achieving full participation and integration of persons with disabilities requires the full cooperation and effort of all TRCC faculty and staff. The college will strive to maintain excellence in its services and to deliver those services equitably and effectively.

Student: Students must complete and submit the form for self-disclosure of a disability to the college Advising and Counseling Center (Room A113) . Students should also contact and meet with a college disability service provider and provide adequate documentation of disability to their disability service provider as soon as possible after admission.

Instructor: As needed, the college disability service provider will interact with faculty to help ensure reasonable and appropriate adjustments for a student with a documented disability. The college disability service provider will complete a memo to faculty and a form detailing appropriate adjustments for the student. Generally, the student will carry this information to instructors and discuss it with them. Whenever possible, the student and faculty member will collaborate on the implementation of the student's adjustments.

The college's two disability service providers are:

Elizabeth Willcox, Advisor
(860) 215-9289, ewillcox@trcc.commnet.edu

Matt Liscum, Counselor
(860)215-9265, mliscum@trcc.commnet.edu

Non-discrimination policy / statement: Three Rivers Community College does not discriminate on the basis of race, color, religious creed, age, sex, national origin, marital status, ancestry, present or past history of mental disorder, learning disability or physical disability, sexual orientation, gender identity and expression, or genetic information in its program and activities. In addition, the College does not discriminate in employment on the basis of veteran status or criminal records. The following person has been designated to handle inquires regarding the non-discrimination policies:

Ken Saad, Equity and Diversity Officer,
(860) 215-9319, KSaad@trcc.commnet.edu

Sexual misconduct policy / statement: Three Rivers Community College strongly encourages all students to report any incidents of sexual misconduct, which includes, but is not limited to, sexual harassment, intimate partner violence, and sexual assault. Students have the right to the prompt and fair resolution of all claims, and the College will preserve the confidentiality of all who report to the fullest extent possible and allowed by law. College employees will explain the limits of confidentiality before information about the incident is revealed. To report sexual misconduct, or to learn more about your options, please contact the Title IX Coordinator. **If you need immediate, confidential assistance, please call the Sexual Assault Crisis Center of Eastern Connecticut (SACCEC) hotline at 860-456-2789**

SACCEC
78 Howard Street, 2nd floor
New London, CT 06320
(860) 442-0604
http://www.saccec.org/

Maria Krug
Title IX Coordinator
Three Rivers Community College
574 New London Turnpike, Norwich, CT 06360
(860) 215-9208; mkrug@trcc.commnet.edu.

TRCC EET Stated Outcomes:

1. Students will practice the skills needed to work effectively in teams and as an individual.
2. Students will demonstrate the ability to use appropriate mathematical and computational skills needed for engineering technology applications.
3. Students will combine oral, graphical, and written communication skills to present and exchange information effectively and to direct technical activities.
4. Students will know of a professional code of ethics.
5. Students will describe concepts relating to quality, timeliness, and continuous improvement.
6. Students will describe how the concepts of electric circuits, electrical measurements, digital electronic devices, programmable logic circuits, electromechanical and automated systems, affect the design, maintenance, and operation of electrical systems.
7. Students will illustrate an ability to think critically and identify, evaluate and solve complex technical and non-technical problems; demonstrate creativity in designing problem solutions; and conduct and interpret experimental data and outcomes.
8. Students will recognize actions and acts of professionalism that allows them to become informed and participating citizens cognizant of ethics, civic duty, and social responsibility.
9. Students will recognize the need to be lifelong learners.

EET K254 Course Outcomes:

1. Convert between binary, decimal, and hexadecimal numbers.
2. Generate the truth table of a given Boolean function.
3. Graphically implement a Boolean function using the appropriate symbols.
4. Use Boolean algebra or Karnaugh maps to simplify a Boolean function with four or less variables.
5. Represent and implement a function in Sum-of-Products (SOP) and Product-of-Sums (POS) form.
6. Explain the difference between positive and negative logic.
7. Explain how a decoder, encoder, multiplexer, & binary adders work.
8. Explain the advantages of using twos complement for binary subtraction.
9. Explain how a sequential device stores data.
10. Draw the generic structure of a sequential circuit.
11. Implement D flip flops as a counter.
12. Implement a state table or diagram using D flip flops, JK flip flops, and combinational components.
13. Explain how tri-state devices are used in a circuit.
14. Given a sequential circuit, analyze the circuit by deriving the flip-flop input and output equations, next state equations, transition table, state table, and state diagram.
15. Given a specification, design a sequential circuit by generating a state diagram, state table, transition table, flip-flop input equations and output equations.
16. Design a combinational and sequential circuit from a customer's specification.
17. Understand and design a sequential circuit using a Algorithmic State Machine.
18. Explain the concept of hierarchical design, including top down and bottom up approaches.
19. Design a sequential circuit clock function.
20. Simulate digital logic circuits on a PC.
21. Program an FPGA using a schematic entry tool.
22. Program an FPGA using Verilog.
23. Explain the purpose of an I/O interface.
24. Develop pseudo-code and a block diagram of the steps to perform an I/O operation using hardware & software.
25. Implement a comparator using combinational logic devices and a register with sequential circuit devices (ICs).
26. Identify the steps to convert an analog signal to a digital signal.
27. Understand the steps that comprise the engineering design process.
28. Successfully design, build, troubleshoot & demonstrate the operation of a digital system that meets customer constraints and maximizes customer provided criteria.
29. Formally document the design and engineering tradeoffs during design and implementation of the product.
30. Formally discuss, explain, and demonstrate the product during a ten minute oral presentation to a technical audience.

Class Policy

Course Web Page: Course material will be posted to Blackboard. The site includes links to a complete syllabus, course schedule, and select homework / quiz / exam solutions. All course announcements including changes to the schedule and modifications to assignments will be made via email announcements.

Schedule: The class schedule, and homework assignments are posted to Blackboard. This will be adjusted as necessary to account for snow days or other unexpected events.

Participation: Every class include a "Peer Time" activity where students work together to solve exercises reinforcing the day's lecture.

Collaboration: Students shall not collaborate on quizzes or exams. Collaboration on homework is allowed and highly encouraged. However, submitted solutions must be independent work.

Homework: Daily homework will be assigned and collected. All homework assignments are due at the beginning of class on the scheduled date. Late homework will be accepted up with a 50% grade penalty. Solutions will be posted to Blackboard. There will be times when the instructor is pressed for time and is unable to carefully grade all homework. Rather than delay grading, only portions of the homework or random student's work will be graded. Items that are not graded are assumed to be correct. Students are encouraged to follow up by comparing their work to the Blackboard posted solutions

Quizzes: There will be at about 10 quizzes this semester (see Blackboard posted schedule). Students, who, in the opinion of the instructor, have a valid excuse will be allowed to take the quiz (including unscheduled) during the instructor's office hours. Others may take the quiz but will have their quiz score multiplied by 0.8. The opportunity to take a quiz ends one week after the quiz is given unless there are extenuating circumstances or other arrangements have been made with the instructor. This allows the instructor to post solutions to Blackboard in a timely manner. Students are allowed to use a single 3 x 5 note card for the quiz. When complete, this card is to be stapled to the quiz. There will be some quizzes where calculators are NOT allowed.

Exams: There will be four in-class examinations (see Blackboard posted schedule). Make up exams are allowed. Student, who in the opinion of the instructor, have a valid excuse will be allowed to take the exam during the instructors office hours. Others may take the exam but will have the exam score multiplied by 0.8. The opportunity to make up an exam ends one week after the exam was given unless there are extenuating circumstances or other arrangements have been made with the instructor. This allows the instructor to post solutions to Blackboard in a timely manner. Students will be allowed to use a single 3 x 5 note card (both sides) and a calculator for all exams. All note cards must be turned in with the exam.

Labs: All labs must be completed to pass this course. Students are responsible for contacting the instructor to make arrangement for a make up lab. At least four of the labs will require a formal written report. Students will be given a rubric for each formal lab report.

Project and Presentation: Students use the final ¼ of this class to design and construct a project showcasing the lessons learned; attendance is mandatory unless prior arrangements have been made with the instructor. Students will present their project to a technical audience on the last day of class.

Assignments and Grading: All problems for quizzes and exams will be graded approximately as described in this rubric:

Percentage	Reflection of content/correctness
100 %	Solution is correct and supporting work is included. Work is clear and concise. When required a clear and concise explanation is given. Drawing and figures are included and properly labeled when required.
80 %	Solution is almost correct but includes a minor computation error copy error, or error in notation. Work is clear and concise. When required clear and concise explanations are given. Drawing and figures are included and properly labeled when required.
60 %	Solution is partially correct but is missing a critical element in the chain of reasoning. When required an explanations is given but may contain flaws in the chain of reasoning. Drawing and figures are included when required but lack a critical element.
40 %	Some understanding of the chain of reasoning is present but the solution incomplete. When required an explanations is given but may contain flaws in the chain of reasoning. Drawing and Figures are not present when required
20 %	Understanding of the chain of reasoning is not demonstrated.
0 %	Work is missing or meaningless.

Extra Credit: Extra credit may be given on rare occasions. All such opportunities will be made available to all students and announced in class or email.

Grade Weight: The class grade is calculated using the following weighting scale:

Item	Weight
Exams	40%
Quizzes	10%
Homework	10%
Formal Labs	10%
Peer Time participation	10%
Project and presentation	20%

The overall grade conversion is:

A+	95% - 100%	A	93% - 94%	A-	90% - 92%
B+	87% - 89%	B	83% - 86%	B-	80% - 82%
C+	77% - 79%	C	73% - 76%	C-	70% - 72%
D+	67% - 69%	D	63% - 66%	D-	60% - 62%
F	0 - 59%				

The class policies and procedures outlined in this document may be changed due to extenuating circumstances or as agreed upon by instructor and students.

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Class #	**Date**	**Quiz / Exam**	**Section Name and Assigned Homework**
1	Wed, August 29		1-1: Digital systems in the world around us 1-2: The world of digital systems 2-4: Introduction to logic gates (brief) 7-4: Off-the-shelf IC types B.2: Real number representation **Homework:** 1.8, 1.11, 1.14, 1.18, 1.21, 1.25, 1.26(A, B, C) Handout (logic families)
-	Mon, September 3	Labor Day	
2	Wed, September 5		1-2: The world of digital systems (review) 2-4 to 2-6: Boolean (part 1 of 3) **Homework:** 1.9, 1.12, 1.15, 1.19, 1.22, 1.27, 1.28 Handout (representation of logic)
3	Mon, September 10	Quiz #1	2-4 to 2-6: Boolean (part 2 of 3) **Homework:** 1.13, 1.16, 1.20 2.3, 2.5 (in term of school busses), 2.10, 2.12
4	Wed, September 12		2-4 to 2-6: Boolean (part 3 of 3) 2-7: Combinational logic design 2-8: More gates **Homework:** 2.35, 2.37, 2.38, 2.45, 2.48, 2.54 2.19, 2.46, 2.51, 2.55, 2.64 Handout (ASCII and microcontrollers)
5	Mon, September 17	Quiz #2	2-9: Decoders and Muxes **Homework:** 2.59, 2.68, 2.71, 2.73, 2.75 Handout
6	Wed, September 19	Exam #1	2-10: Additional considerations 6-2: K-maps (part 1 of 2) **Homework:** 2.77, 2.78, 6.1, 6.3, 6.5 Handout

Class #	Date	Quiz / Exam	Section Name and Assigned Homework
7	Mon, September 24		6-2: K-maps (part 2 of 2) **Homework:** 6.2, 6.4, 6.8, 6.10 Handout
8	Wed, September 26	Quiz #3	3-2: Storing one bit (part 1 of 2) **Homework:** 3.1, 3.10, 3.16, 3.17 Handout
9	Mon, October 1		3-2: Storing one bit (part 2 of 2) **Homework:** 3.2, 3.5, 3.11, 3.20 Handout
10	Wed, October 3	Quiz #4	3-3: (FSM part 1 of 2) 3-5: More on Flip-Flops and Controllers **Homework:** 3.3, 3.23, 3.25 Handout
11	Mon, October 8	Exam #2	3-3: (FSM part 2 of 2) **Homework:** 3.22, 3.25, 3.28 Handout

Class #	Date	Quiz / Exam	Section Name and Assigned Homework
12	Wed, October 10		Introduction to the FPGA (Schematic entry) Overview of microcontroller **Homework:** Handout
13	Mon, October 15	Quiz #4	4-2: Registers **Homework:** 4.1, 4.3, 4.6 Handout
14	Wed, October 17		4-3: Adders 4-4: Comparators **Homework:** 4.2, 4.7, 4.8, 4.9, 4.11, 4.14 Handout
15	Mon, October 22	Quiz #5	4-3 Shifters 4-5: Multiplier 4-6: Subtractors **Homework:** 4.10, 4.15, 4.29, 4.31, 4.33, 4.36, 4.43 Handout
16	Wed, October 24	Exam #3	4-7: Arithmetic-Logic Units 4-6: Subtractors **Homework:** 4.28, 4.32, 4.34. 4.40 Handout

Class #	Date	Quiz / Exam	Section Name and Assigned Homework
17	Mon, October 29		9-2 Hardware Description Language **Homework:** 9.1, 9.3, 9.5, 9.7, 9.9 Handout
18	Wed, October 31	Quiz #6	9-3 Sequential logic **Homework:** 9.2, 9.4, 9.6, 9.11, 9.13 Handout
19	Mon, November 5		5-2: High-level state machines **Homework:** 9.12, 5.1, 5.3, 5.5 Handout
20	Wed, November 7	Quiz #7	6-3: Moore verses Mealy FSM 5-3: RTL Design Process Homework: **Handout**
21	Mon, November 12	Exam #4	Project

Class #	Date	Quiz / Exam	Section Name and Assigned Homework
22	Wed, November 14		Project
23	Mon, November 19	Quiz #8	Project
24	Wed, November 21		Project
25	Mon, November 26	Quiz #9	Project
26	Wed, November 28		Project
27	Mon, December 3		Project
28	Wed, December 5	Quiz #10	Project
29	Mon, December 10		Project
30	Wed, December 12		Presentation