Tentative Syllabus: Fall '10
Digital Electronics I
Prof. Rhoades

Sequence	Topic	Text Chapter	Chapter Sections	Comments
I.	Introduction	1	1-5	Overview, etc.
II.	Binary-number Arithmetic	2	1-7	Floating-point overview only (with offset-binary).
III.	Other Codes	2	8, 10-12	Hamming code overview only.
IV.	Basic Logic Gates	3	1-3	NOT, AND, OR. Test 1
V.	Other Logic Gates	3, 14 (as ref.)	4-6, 8	NAND, NOR, XOR, XNOR, logic families
VI.	Logic Simplification	4	1-9, (10)	Emphasize SOP form.
VII.	Combinational Logic Circuits	5	1-5	Emphasize NANDs Test 2
VIII.	Combinational Logic Functions	6	1-5, 8-10	Adder, MUX, etc.
IX.	Sequential Logic	7	1-4, (5-6)	Memory devices: Latch, Flip-flops, etc.
X.	Counters	8	1-2, (3), 4, (5-7)	Types of counters and sequences.
XI.	Shift Registers	9	1, (2-5)	Principles. Test 3

Text: Floyd, *Digital Fundamentals*, 10th edition.
Class: Room E204, Tues/Thurs. 1:00-2:15 p.m. No class 11/11 or 11/25, optional makeup day 11/23 (12/17, 12/20 if needed).
Office: Room C232 (office hours MW 2:00-3:20).

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Week	Date	Title
L1	8/31/10	Logic Gate Characteristics
L2	9/7/10	Signed and Unsigned Binary Math
L3	9/14/10	Basic Logic Design
L4	9/21/10	Stop Light
L5	9/28/10	Binary Counter to BCD Converter
L6	10/5/10	↓
L7	10/12/10	Adders and Comparators
L8	10/19/10	↓
L9	10/26/10	Data Selector and Decoder Functions (D Flip-Flop)
L10	11/2/10	↓
L11	11/9/10	Parallel and Serial Parity Circuits (Shift Register)
L12	11/16/10	↓
L13	11/30/10	Counters (J-K Flip-Flops)
L14	12/7/10	↓
L15	12/14/10	Only if needed for makeup

Note: Lab meets in Room B213, Tues. 5:00-7:45 p.m. Optional makeup day: 11/23/10.
Office: Room C232 (office hours MW 2:00-3:20).