Tentative Syllabus: Fall '13
Digital Electronics I
Prof. Rhoades

Sequence	Topic	Text Chapter	Chapter Sections	Comments
I.	Introduction	1	1-5	Overview, etc.
II.	Binary-number Arithmetic	2	1-7	Floating-point overview only (with offset-binary).
III.	Other Codes	2	8, 10-12	Cyclic redundancy check overview only.
IV.	Basic Logic Gates	3	1-3	NOT, AND, OR. Test 1
V.	Other Logic Gates	3, 14 (as ref.)	4-6, 8	NAND, NOR, XOR, XNOR, logic families
VI.	Logic Simplification	4	1-9, (10)	Emphasize SOP form.
VII.	Combinational Logic Circuits	5	1-5	Emphasize NANDs Test 2
VIII.	Combinational Logic Functions	6	1-5, 8-10	Adder, MUX, etc.
IX.	Sequential Logic	7	1-4, (5-6)	Memory devices: Latch, Flip-flops, etc.
X.	Counters	8	1-2, (3), 4, (5-7)	Types of counters and sequences.
XI.	Shift Registers	9	1, (2-5)	Principles. Test 3

Text: Floyd, *Digital Fundamentals*, 10th edition.
Class: Room D126, T & Th. 1:00-2:15 p.m. No class 11/28/13.
Optional makeup days: 11/26/13, 12/19/13.
Office: Room C232 (M & W 1:00-1:50, T 12:00-12:50).

Tests: Tests count part of the course grade, probably three tests as shown above.

Project: A project TBD may be assigned, worth part of the course grade. This could be a research paper, design problem, etc.

Homework: Worth part of the course grade. A few assignments will be collected, unannounced, for assessment. Also, each student, at random, will present the solution to a selected problem before the instructor's solution is revealed.

Lab Grade: This will be determined this semester by John Forella. We may or may not combine lecture and lab grades TBD. See the separate lab syllabus for details.

Academic Honesty

Students are expected to follow College policy on Academic Honesty regarding assignments. Specifically, be aware of the difference between collaboration and copying and be careful to cite sources when required. This policy also includes expectation of regular class attendance, punctuality, and timeliness in completing assignments.

College Withdrawal Policy

Students may withdraw, in writing or verbally at the Registrar's Office for any reason until the end of the 10th week of classes. From the 11th week through the end of the 13th week, a student may withdraw with the instructor's written approval.

Disabilities Statement

If you are a student with a disability and believe you will need accommodations for this class, it is your responsibility to contact the Disabilities Counseling Services at 383-5240. To avoid any delay in the receipt of accommodations, you should contact the counselor as soon as possible. Please note that I cannot provide accommodations based upon disability until I have received an accommodation letter from the Disabilities Counselor.

Course Outcomes

ABET Outcome Requirements– Associate Degree Programs - 2013/2014

a. an ability to apply the knowledge, techniques, skills, and modern tools of the discipline to narrowly defined engineering technology activities;
b. an ability to apply a knowledge of mathematics, science, engineering, and technology to engineering technology problems that require limited application of principles but extensive practical knowledge;
c. an ability to conduct standard tests and measurements, and to conduct, analyze, and interpret experiments;
d. an ability to function effectively as a member of a technical team;
e. an ability to identify, analyze, and solve narrowly defined engineering technology problems;
f. an ability to apply written, oral, and graphical communication in both technical and nontechnical environments; and an ability to identify and use appropriate technical literature;
g. an understanding of the need for and an ability to engage in self-directed continuing professional development;
h. an understanding of and a commitment to address professional and ethical responsibilities, including a respect for diversity; and
i. a commitment to quality, timeliness, and continuous improvement.

TRCC EET Stated Outcomes

1. Students will practice the skills needed to work effectively in teams and as an individual.
2. Students will demonstrate the ability to use appropriate mathematical and computational skills needed for engineering technology applications.
3. Students will combine oral, graphical, and written communication skills to present and exchange information effectively and to direct technical activities.
4. Students will know of a professional code of ethics.
5. Students will describe concepts relating to quality, timeliness, and continuous improvement.
6. Students will describe how the concepts of electric circuits, electrical measurements, digital electronic devices, programmable logic circuits, electromechanical and automated systems, affect the design, maintenance, and operation of electrical systems.
7. Students will illustrate an ability to think critically and identify, evaluate and solve complex technical and non-technical problems; demonstrate creativity in designing problem solutions; and conduct and interpret experimental data and outcomes.
8. Students will recognize actions and acts of professionalism that allows them to become informed and participating citizens cognizant of ethics, civic duty, and social responsibility.
9. Students will recognize the need to be lifelong learners.

K254/5 Course Outcomes

1. Mastery of Electrical Technology concepts as defined in the course syllabus
2. Knowledge of unsigned and signed binary number systems and associated arithmetic, including the hexadecimal and binary-coded decimal systems.
3. Knowledge of concepts of combinational and sequential logic.
4. Demonstrate an ability to build and test circuits and systems related to digital electronics
5. Demonstrate an ability to analyze and solve problems related to digital electronics
6. Demonstrate senior level oral and written communication skills
7. Demonstrate an appreciation for lifelong learning
8. Demonstrate proper professional and ethical behavior
9. Demonstrate a commitment to quality, timeliness and continuous improvement

Tentative Syllabus: Fall 2013
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Week	Date (2013)	Title
–	8/29	Introduction
L1	9/3 & 5	Logic Gate Characteristics
L2	9/10 & 12	Signed and Unsigned Binary Math (MultiSim)
L3	9/17 & 19	Basic Logic Design
L4	9/24 & 26	Stop Light
L5	10/1 & 3	Binary Counter to BCD Converter
L6	10/8 & 10	↓
L7	10/15 & 17	Adders and Comparators
L8	10/22 & 24	↓
L9	10/29 & 31	Data Selector and Decoder Functions (D Flip-Flop)
L10	11/5 & 7	↓
L11	11/12 & 14	Parallel and Serial Parity Circuits (Shift Register)
L12	11/19 & 21	↓
L13	12/3 & 5	Counters (J-K Flip-Flops)
L14	12/10, 12, 17	Only if needed for makeup

Note: Lab meets in Room B229, T & Th. 2:16-3:30 p.m. No class 11/28/13.
Optional makeup days: 11/26/13, 12/19/13.
Office: Room C232 (M & W 1:00-1:50, T 12:00-12:50).

Note: Lab breadboards will be signed out for the semester (one per group per course) and may be kept in the workbench drawers. There will be labels available. They ***must*** be signed back in at the end of the semester.