Tentative Syllabus: Fall '07
Digital Electronics I
Prof. Rhoades

Sequence	Topic	Text Chapter	Chapter Sections	Comments
I.	Introduction	1	1-5	Overview, etc.
II.	Binary-number Arithmetic	2	1-7	Floating-point overview only (with offset-binary).
III.	Other Codes	2	8, 10-12	Hamming code overview only.
IV.	Basic Logic Gates	3	1-3	NOT, AND, OR. Test 1
V.	Other Logic Gates	3, 14 (as ref.)	4-6, 8	NAND, NOR, XOR, XNOR, logic families
VI.	Logic Simplification	4	1-9, (10)	Emphasize SOP form.
VII.	Combinational Logic Circuits	5	1-5	Emphasize NANDs Test 2
VIII.	Combinational Logic Functions	6	1-5, 8-10	Adder, MUX, etc.
IX.	Sequential Logic	7	1-4, (5-6)	Memory devices: Latch, Flip-flops, etc.
X.	Counters	8	1-2, (3), 4, (5-7)	Types of counters and sequences.
XI.	Shift Registers	9	1, (2-5)	Principles. Test 3

Text: Floyd, *Digital Fundamentals*, 9th edition.
Class: Room 105 Thames, MWF 12:30-1:20 p.m.
Office: Room 124 Thames (office hours TBA).

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Week	Date	Title
L1	8/30/07	Logic Gate Characteristics
L2	9/6/07	Signed and Unsigned Binary Math
L3	9/13/07	Basic Logic Design
L4	9/20/07	Stop Light
L5	9/27/07	Binary Counter to BCD Converter
L6	10/4/07	↓
L7	10/11/07	Adders and Comparators
L8	10/18/07	↓
L9	10/25/07	Data Selector and Decoder Functions (D Flip-Flop)
L10	11/1/07	↓
L11	11/8/07	Parallel and Serial Parity Circuits (Shift Register)
L12	11/15/07	↓
L13	11/29/07	Counters (J-K Flip-Flops)
L14	12/6/07	↓
L15	12/13/07	Final Exam Period (only if needed for makeup)

Note: Lab meets in Room 117 Thames, Thurs. 1:30-4:20 p.m.